



GL100J65A47P

GL Silicon N-Channel Super-Junction Power MOSFET

General Description

GL100J65A47P the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned Super-junction Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247PLUS, which accords with the RoHS standard.

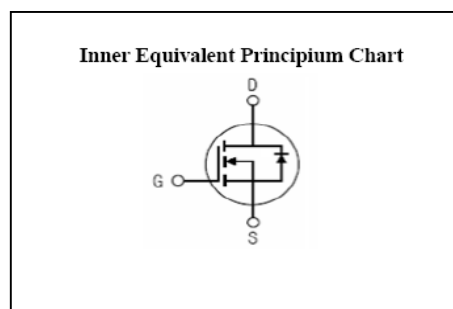
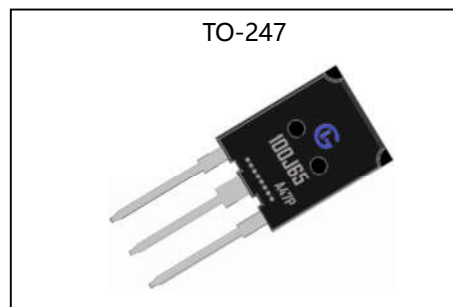
V_{DSS}	650	V
I_D	100	A
$P_D(T_C=25^{\circ}C)$	625	W
$R_{DS(ON)TYP}$	18	m Ω

Features

- Fast Switching
- Low Gate Charge and Rdson
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)



Absolute (Tc= 25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	100	A
I_{DM}^{a1}	Pulsed Drain Current	400	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	3100	mJ
P_D	Power Dissipation	625	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^{\circ}C$
T_L	Maximum Temperature for Soldering	300	$^{\circ}C$

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	0.2	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-Ambient	30	$^{\circ}C/W$



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Electrical Characteristics (Tc= 25°C unless otherwise specified)

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	650	--	--	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} =650V, V _{GS} =0V, T _a =25°C	--	--	10	μA
		V _{DS} =520V, V _{GS} =0V, T _a =150°C	--	--	100	
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} = +30V	--	--	100	nA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} = -30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)} ^{a3}	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =50A	--	18	22	mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	3.0	--	5.0	V

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs} ^{a3}	Forward Transconductance	V _{DS} =10V, I _D =50A	--	75	--	S
C _{iss}	Input Capacitance	V _{GS} =0V, V _D =25V f=1.0MHz	--	15600	--	pF
C _{oss}	Output Capacitance		--	380	--	
C _{rss}	Reverse Transfer Capacitance		--	14	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =350V, I _D =50A, V _{GS} =10V, R _g =2Ω	--	230	--	ns
t _r	Rise Time		--	90	--	
t _{d(OFF)}	Turn-Off Delay Time		--	190	--	
t _f	Fall Time		--	90	--	
Q _g	Total Gate Charge	V _{DD} =350V, I _D =50A V _{GS} =0 to 10V	--	350	--	nC
Q _{gs}	Gate to Source Charge		--	90	--	
Q _{gd}	Gate to Drain ("Miller") Charge		--	120	--	

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Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	100	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	400	A
V_{SD}	Diode Forward Voltage	$I_S=100A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=50A, V_{GS}=0V$	--	280	--	ns
Q_{rr}	Reverse Recovery Charge	$I_S=I_F, d_i/d_t=100A/\mu s$	--	1.5	--	μC

Pulse width $t_p \leq 380\mu s, \delta \leq 2\%$

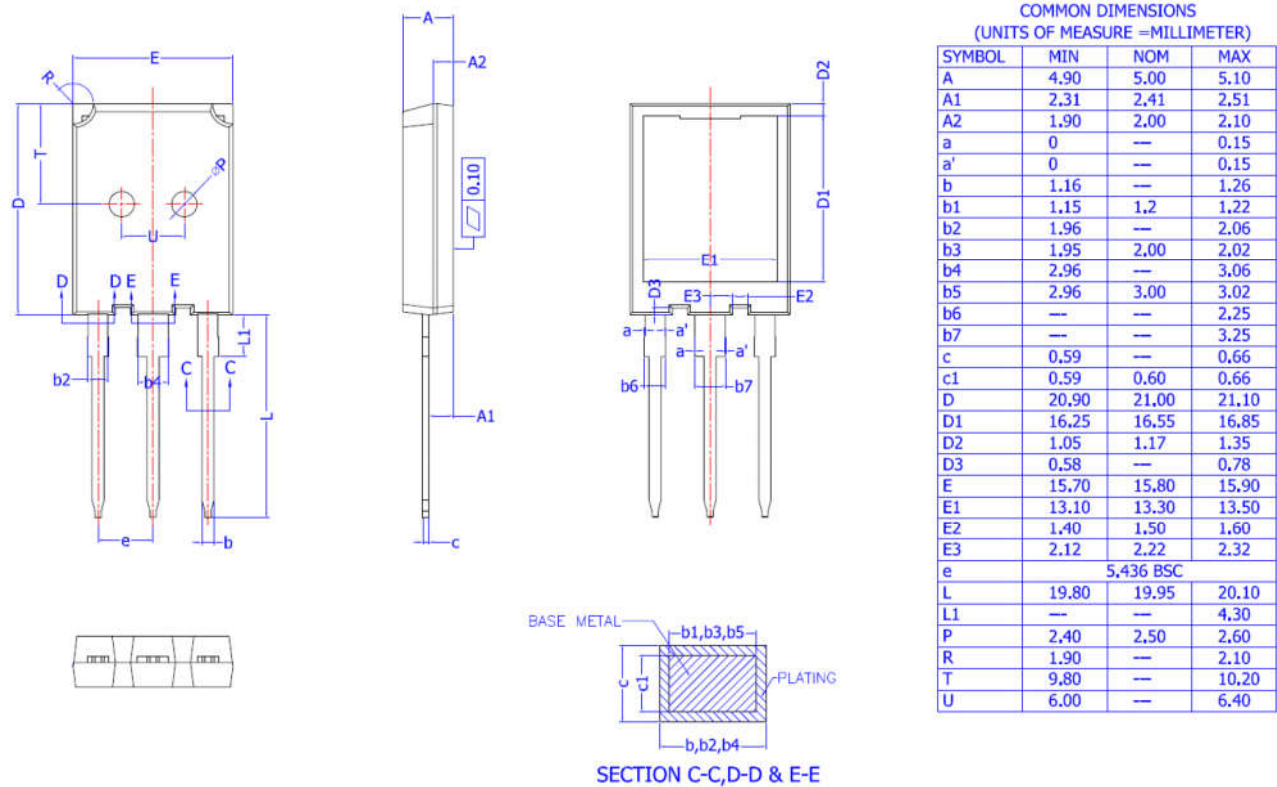
a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $I_{AS}=100A, V_{DD}=50V, R_G=25\Omega$, Starting $T_J=25^\circ C$

a3: Pulse Test: Pulse width $\leq 380\mu s$, Duty Cycle $\leq 2\%$

Package mechanical data

Figure 1



Typical Characteristics

Figure 2. Safe operating area

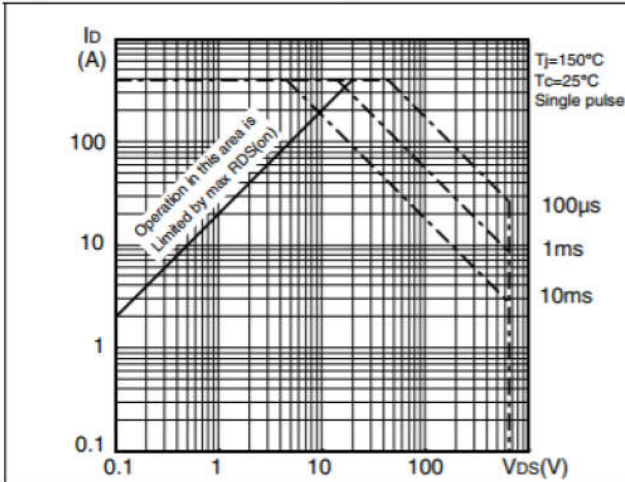


Figure 3. Thermal impedance

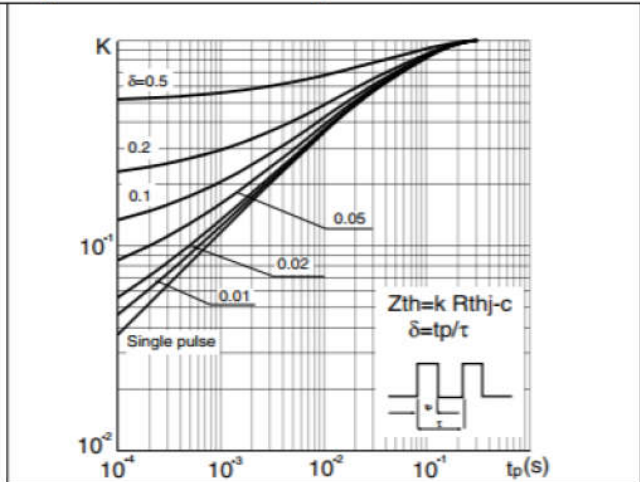


Figure 4. Output characteristics

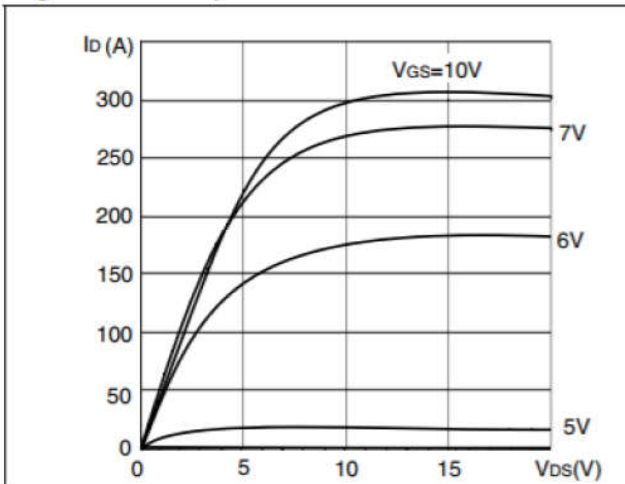


Figure 5. Transfer characteristics

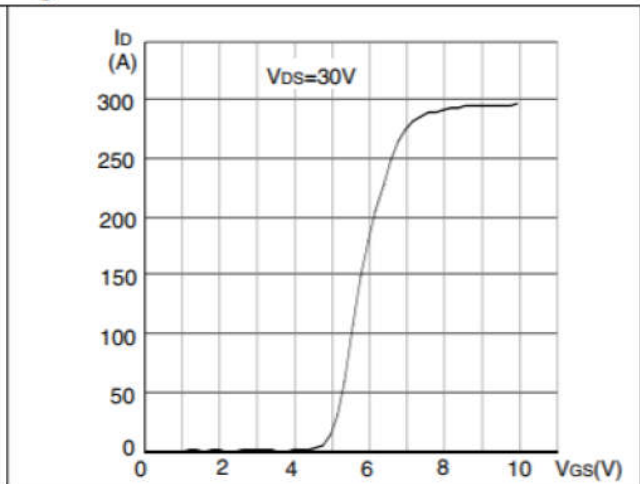


Figure 6. Normalized VDS vs temperature

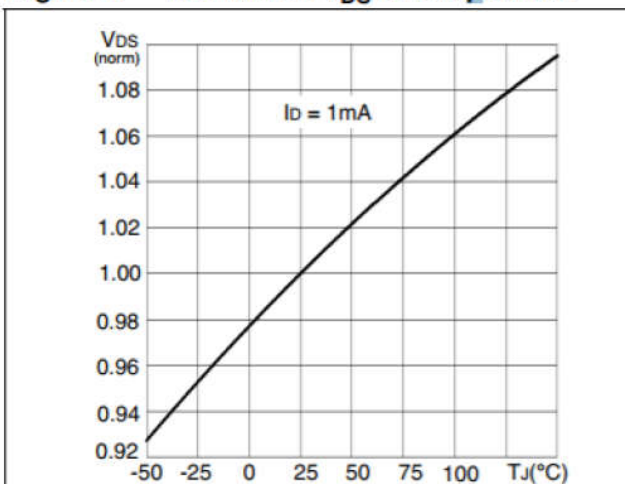
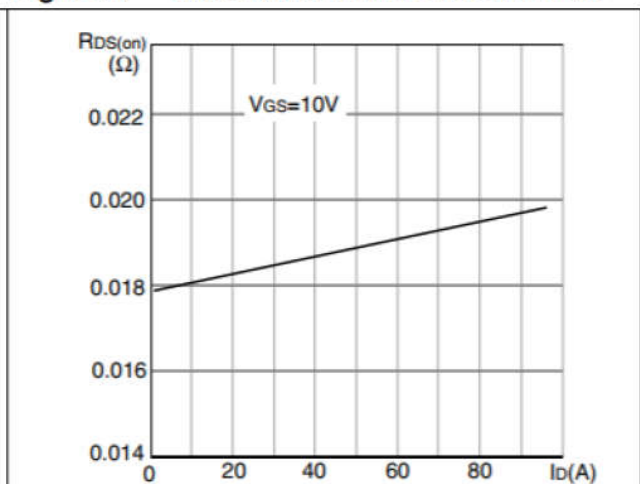


Figure 7. Static drain-source on resistance



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Figure 8. Gate charge vs gate-source voltage **Figure 9. Capacitance variations**

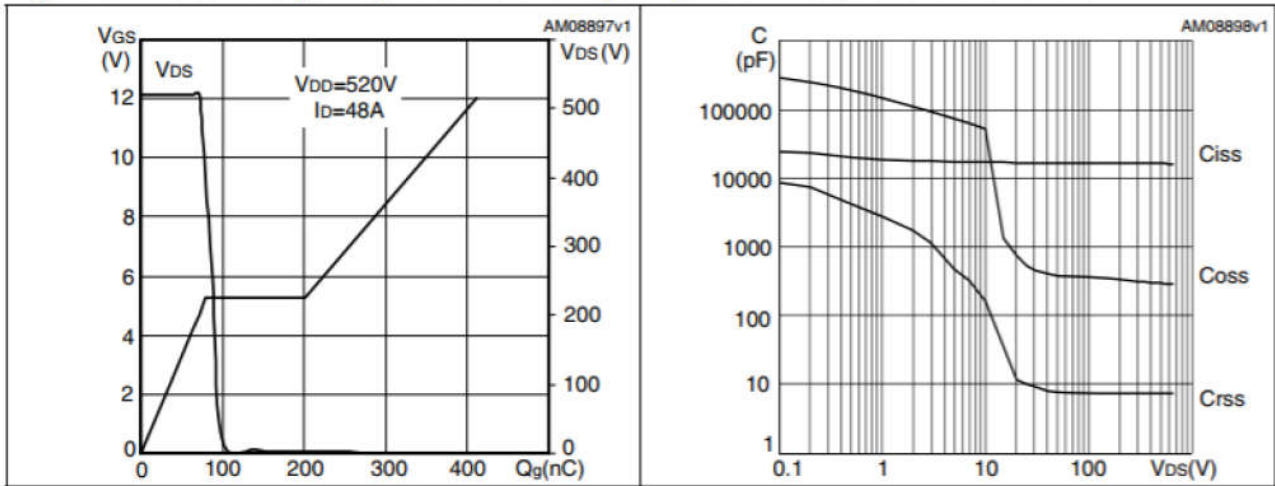


Figure 10. Normalized gate threshold voltage vs temperature **Figure 11. Normalized on resistance vs temperature**

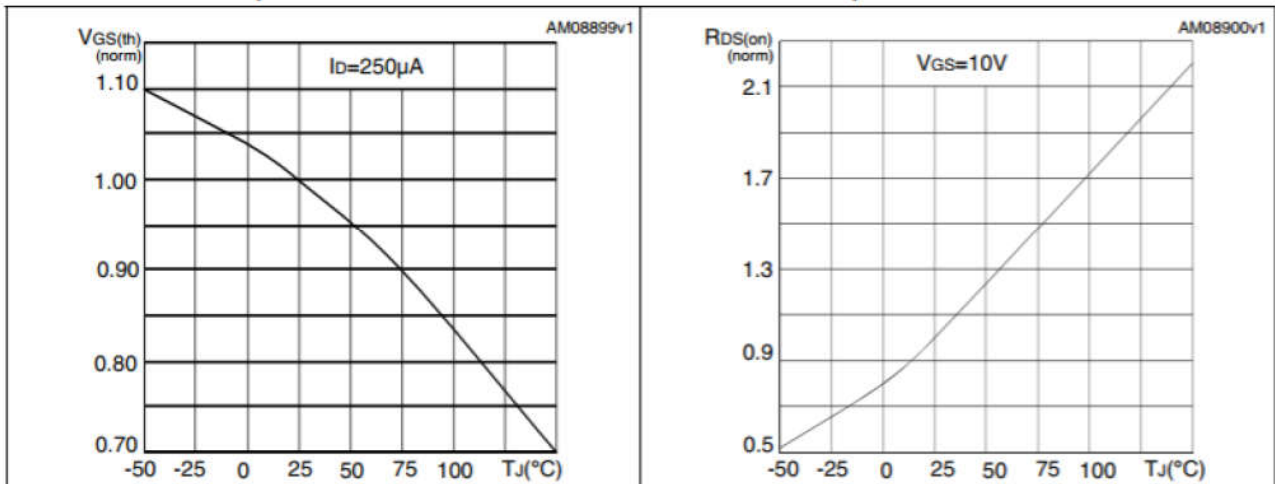


Figure 12. Output capacitance stored energy **Figure 13. Switching losses vs gate resistance (1)**

