



GL65R300FA9

GL Silicon N-Channel Super-Junction Power MOSFET

General Description

GL65R300FA9 the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned Super-junction Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

Features

- Fast Switching
- Low Gate Charge and Rdson
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)

Absolute (Tc= 25°C unless otherwise specified)

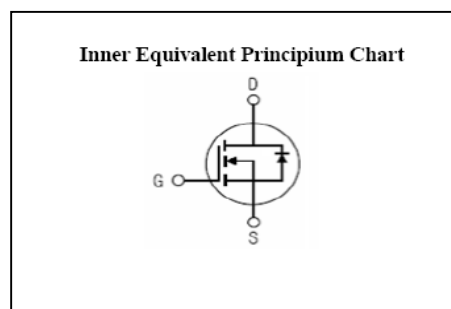
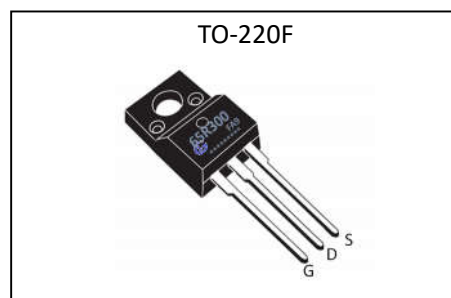
Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage	650	V
I _D	Continuous Drain Current	15	A
I _{DM} ^{a1}	Pulsed Drain Current	60	A
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS} ^{a2}	Single Pulse Avalanche Energy	130	mJ
P _D	Power Dissipation	34	W
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	300	°C

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Typ.	Units
R _{θJC}	Junction-to-Case	3.67	°C/W
R _{θJA}	Junction-to-Ambient	100	°C/W

V _{DSS}	650	V
I _D	15	A
P _D (T _C =25°C)	34	W
R _{DS(ON)TYP}	0.27	Ω





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Electrical Characteristics (Tc= 25°C unless otherwise specified)

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=650V, V_{GS}=0V, T_a=25^\circ C$	--	--	1.0	μA
		$V_{DS}=520V, V_{GS}=0V, T_a=125^\circ C$	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}^{a3}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=7A$	--	0.27	0.31	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	--	4.5	V

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}^{a3}	Forward Transconductance	$V_{DS}=10V, I_D=7A$	--	11	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V, V_D=50V$ $f=1.0MHz$	--	630	--	pF
C_{oss}	Output Capacitance		--	54	--	
C_{rss}	Reverse Transfer Capacitance		--	32	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=400V, I_D=7A,$ $V_{GS}=10V, R_g=10\Omega$	--	113	--	ns
t_r	Rise Time		--	15	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	50	--	
t_f	Fall Time		--	17	--	
Q_g	Total Gate Charge	$I_D=7A, V_{DD}=480V$ $V_{GS}=0 \text{ to } 10V$	--	33	--	nC
Q_{gs}	Gate to Source Charge		--	8	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	15	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current(Body Diode)		--	--	15	A
I_{SM}	Maximum Pulsed Current(Body Diode)		--	--	60	A
V_{SD}	Diode Forward Voltage	$I_S=15A, V_{GS}=0V$	--	0.82	1.5	V
t_{rr}	Reverse Recovery Time	$V_R=480V, V_{GS}=0V$	--	250	--	ns
Q_{rr}	Reverse Recovery Charge	$I_S=I_F, d_i/d_t=100A/us,$	--	2.2	--	uC

Pulse width $t_p \leq 380\mu s, \delta \leq 2\%$

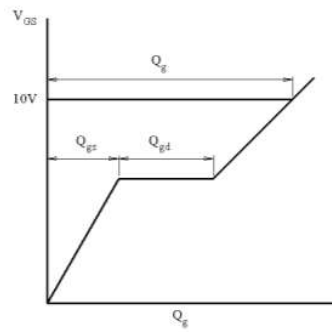
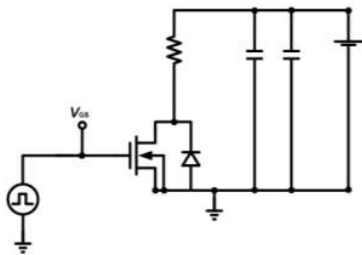
a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $L=10mH, V_{DD}=50V$, Starting $T_J=25^\circ C$

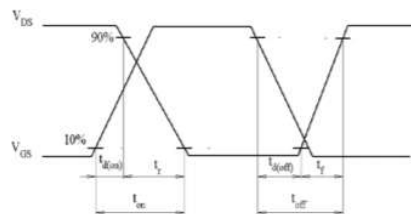
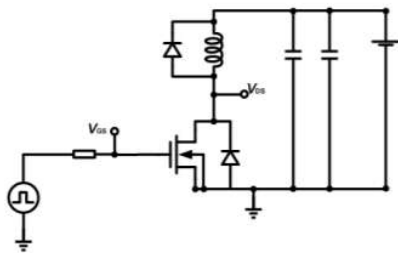
a3: Pulse Test: Pulse width $\leq 380\mu s$, Duty Cycle $\leq 2\%$

Test Circuits

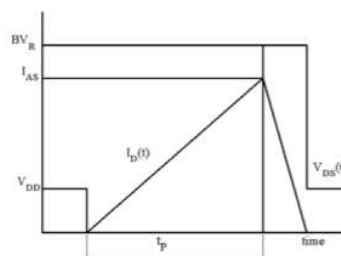
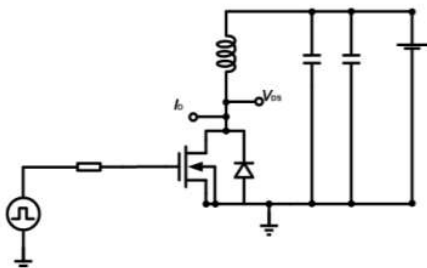
1. Gate Charge Test Circuit & Waveform



2. Switch Time Test Circuit

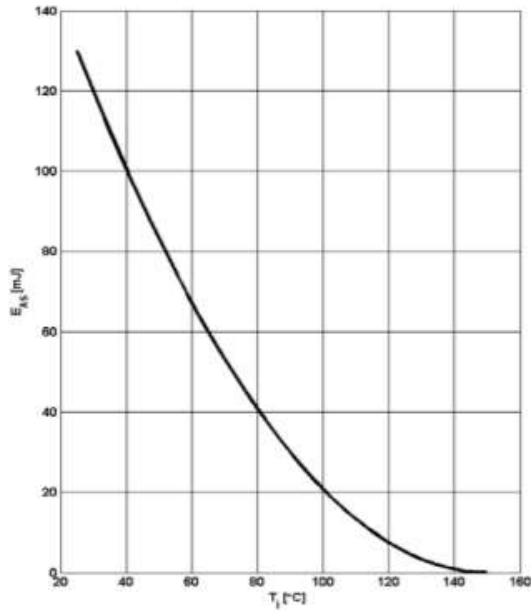


3. Unclaimed Inductive Switching Test Circuit & Waveforms



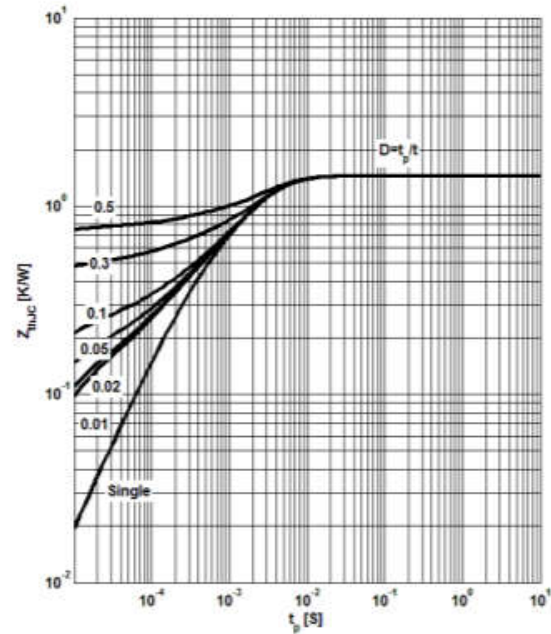
Typical Characteristics

Figure 3: Power Dissipation



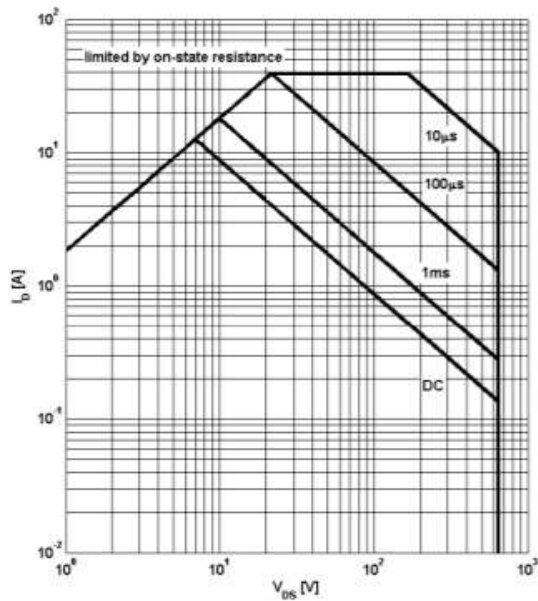
$$P_{\text{tot}} = f(T_c)$$

Figure 4: Max. Transient Thermal Impedance



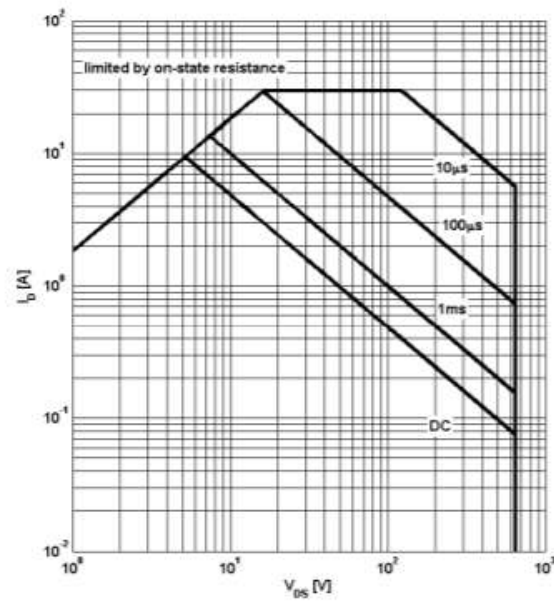
$$Z_{\text{thJC}} = f(t_p); \text{ parameter: } D = t_p/T$$

Figure 5: Safe Operating Area



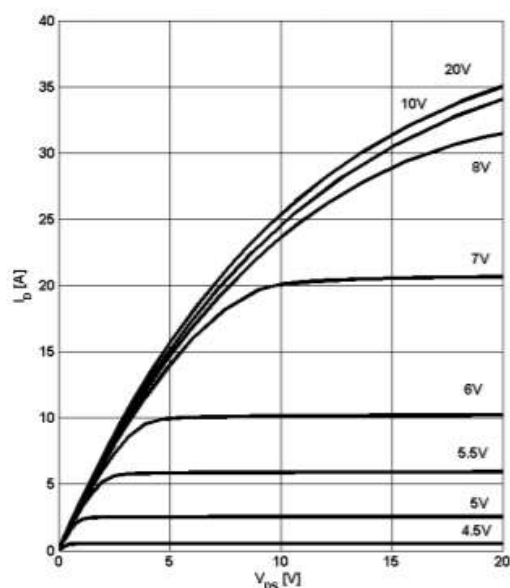
$$I_D = f(V_{DS}); T_c = 25^\circ\text{C}; V_{GS} > 7\text{V}; \text{ parameter } t_p$$

Figure 6: Safe Operating Area



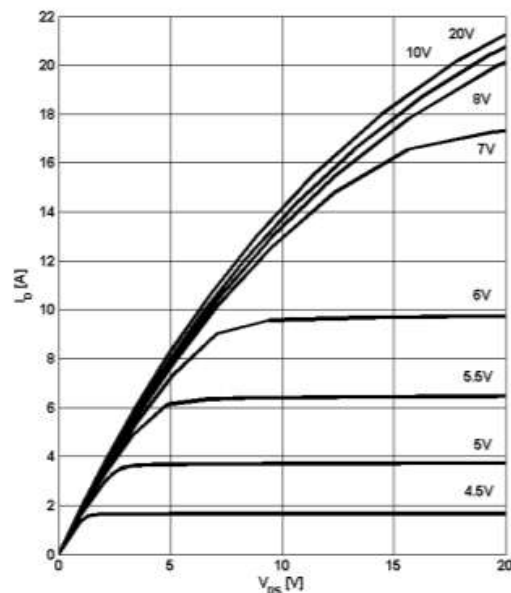
$$I_D = f(V_{DS}); T_c = 80^\circ\text{C}; V_{GS} > 7\text{V}; \text{ parameter } t_p$$

Figure 7: Typ. Output Characteristics



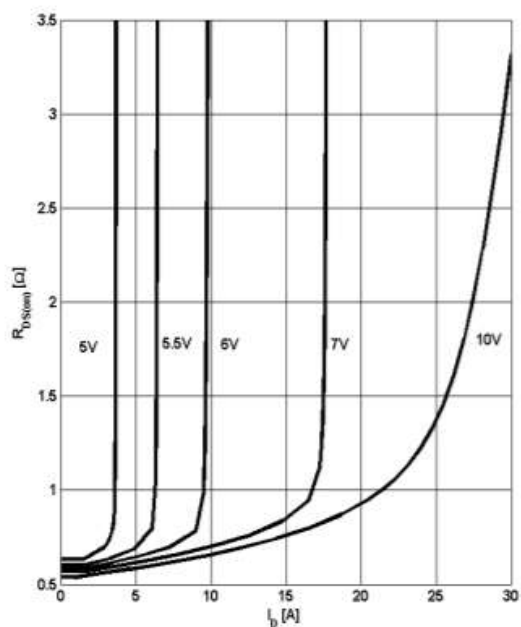
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Figure 8: Typ. Output Characteristics



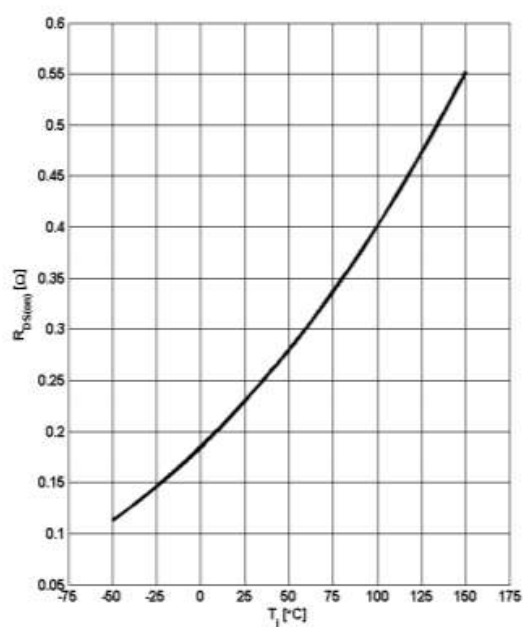
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Figure 9: Typ. Drain-Source On-State Resistance



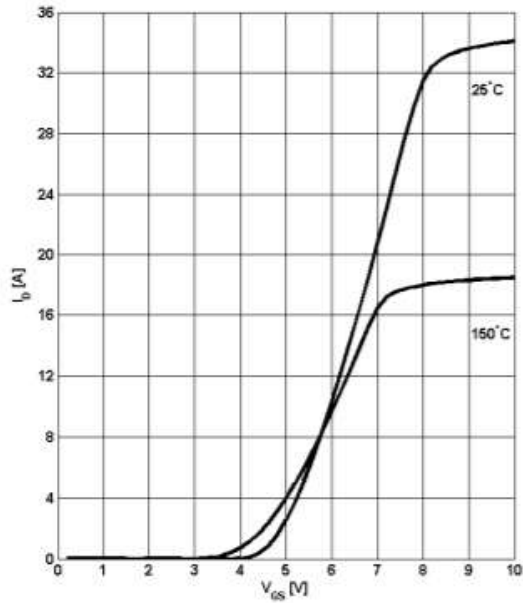
$R_{DS(ON)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Figure 10: Typ. Drain-Source On-State Resistance



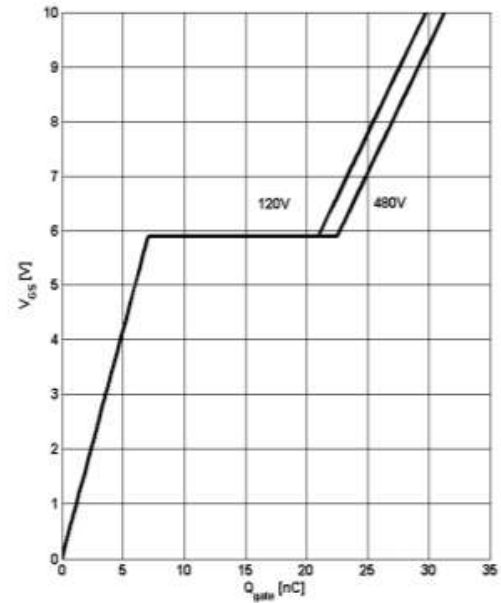
$R_{DS(ON)} = f(T_j)$; $I_D = 7.0\text{A}$; $V_{GS} = 10\text{V}$

Figure 11: Typ. Transfer Characteristics



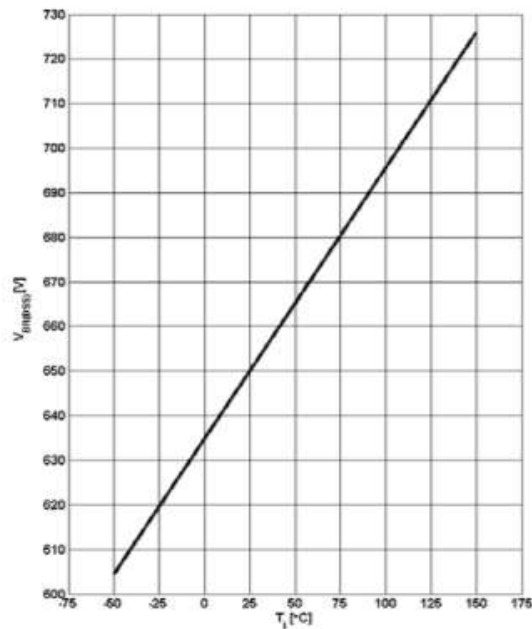
$$I_D = f(V_{GS}); V_{DS} = 20V$$

Figure 12: Typ. Gate Charge



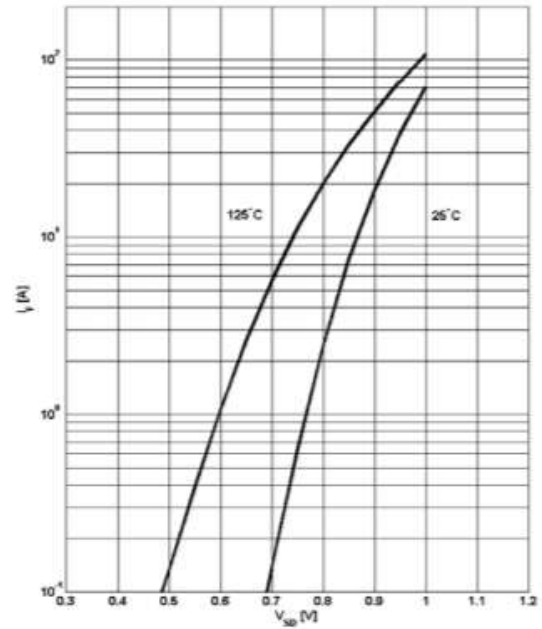
$$V_{GS} = f(Q_{gate}), I_D = 5.0A \text{ pulsed}$$

Figure 13: Drain-Source Breakdown Voltage



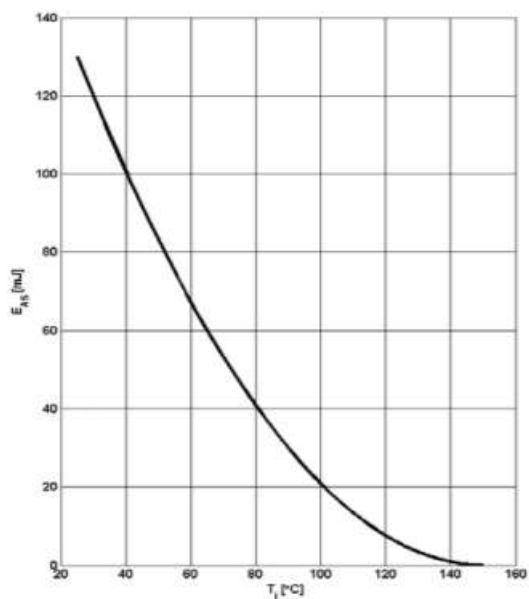
$$V_{BR(DSS)} = f(T_j); I_D = 1mA$$

Figure 14: Forward Characteristics of Reverse Diode



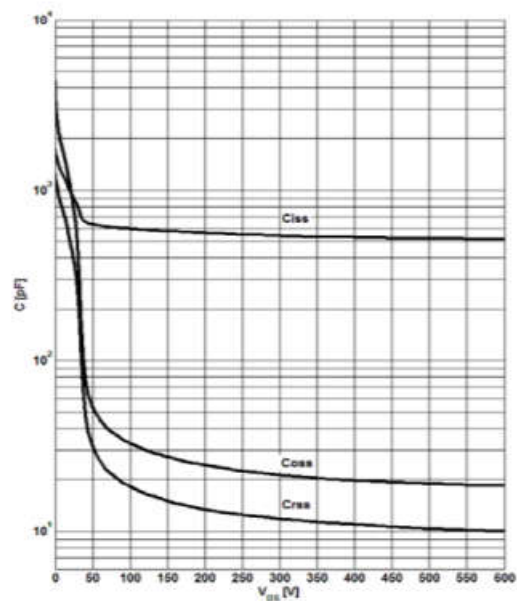
$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Figure 15: Avalanche Energy



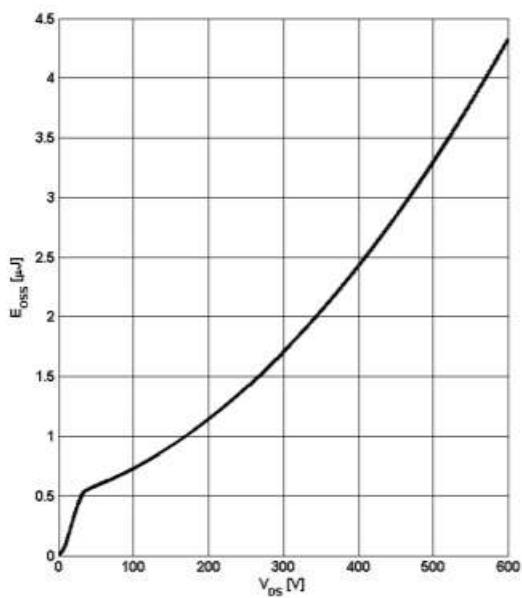
$$E_{AS}=f(T_J); I_D=1.7A; V_{DD}=60V$$

Figure 16: Typ. Capacitances



$$C=f(V_{DS}); V_{GS}=0; f=1MHz$$

Figure 17: C_{OSS} Stored Energy



$$E_{OSS}=f(V_{DS})$$