GL65R300A4

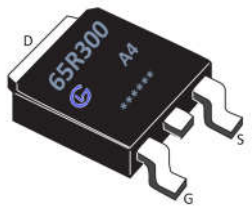
GL Silicon N-Channel Super-Junction Power MOSFET

V_{DSS}	650	V
I_D	15	A
$P_D(T_C=25℃)$	65	W
$R_{DS(ON)TYP}$	0.29	Ω

General Description

GL65R300A4 the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned Super-Junction Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

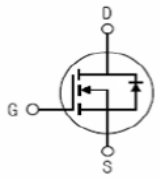
TO-252



Features

- Fast Switching
- Low Gate Charge and Rdson
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)

Absolute (Tc= 25℃ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	15	A
I_{DM}[a1]	Pulsed Drain Current	60	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	130	mJ
P_D	Power Dissipation	65	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, −55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	1.92	℃/W
$R_{\theta JA}$	Junction-to-Ambient	100	℃/W

Electrical Characteristics (Tc= 25℃ unless otherwise specified)

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	650	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=650V,V_{GS}= 0V,T_a=25℃	--	--	1.0	μA
		V_{DS}=520V,V_{GS}=0V,T_a=125℃	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$[a3]	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=7.5A	--	0.29	0.33	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.5	--	4.5	V

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}[a3]	Forward Transconductance	V_{DS}=10V,I_D=7A	--	11	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_D=50V f=1.0MHz	--	630	--	pF
C_{oss}	Output Capacitance		--	54	--	
C_{rss}	Reverse Transfer Capacitance		--	32	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=400V,I_D=7A, V_{GS}=10V,R_g=10Ω	--	113	--	ns
t_r	Rise Time		--	15	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	50	--	
t_f	Fall Time		--	17	--	
Q_g	Total Gate Charge	I_D=7A,V_{DD}=480V V_{GS}=0 to 10V	--	33	--	nC
Q_{gs}	Gate to Source Charge		--	8	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	15	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current(Body Diode)		--	--	15	A
I_{SM}	Maximum Pulsed Current(Body Diode)		--	--	60	A
V_{SD}	Diode Forward Voltage	I_S=15A,V_{GS}=0V	--	0.82	1.5	V
t_{rr}	Reverse Recovery Time	V_R=480V,V_{GS}=0V	--	250	--	ns
Q_{rr}	Reverse Recovery Charge	I_S=I_F,d_i/d_t=100A/us,	--	2.2	--	uC
Pulse width tp≤380μs,δ≤2%						

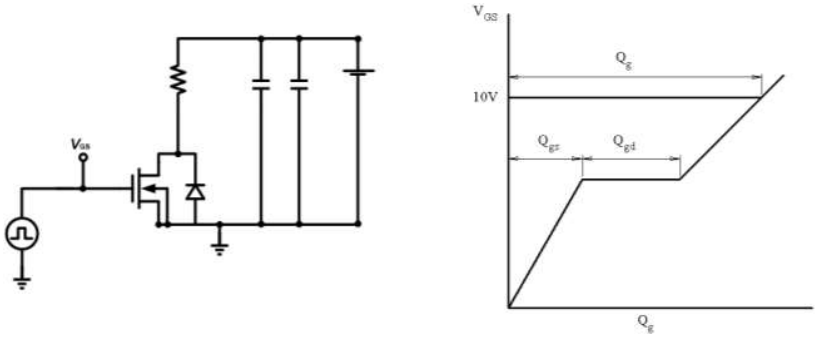
[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: L=10mH,V_{DD}=50V, Starting T_J=25°C

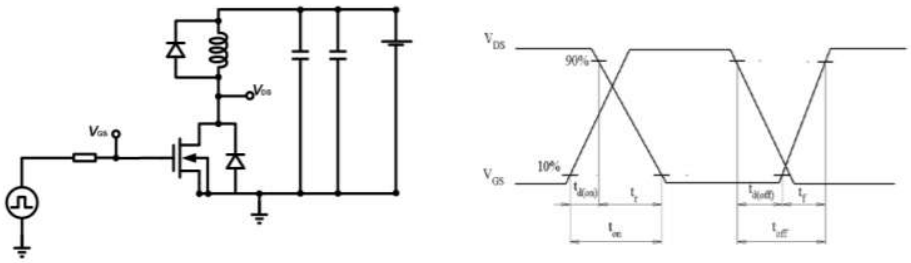
[a3]: Pulse Test: Pulse width≤380us, Duty Cycle≤ 2%

Test Circuits

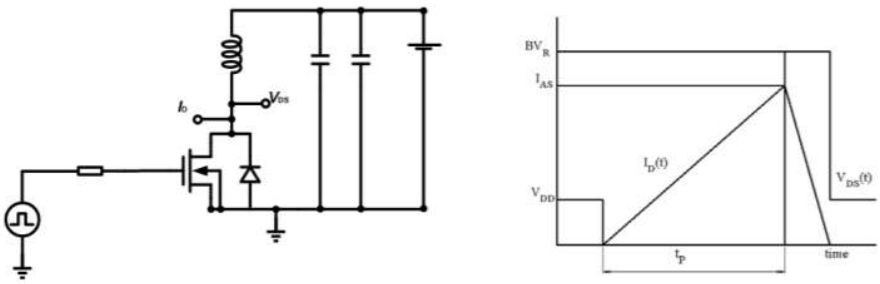
1. Gate Charge Test Circuit & Waveform



2. Switch Time Test Circuit

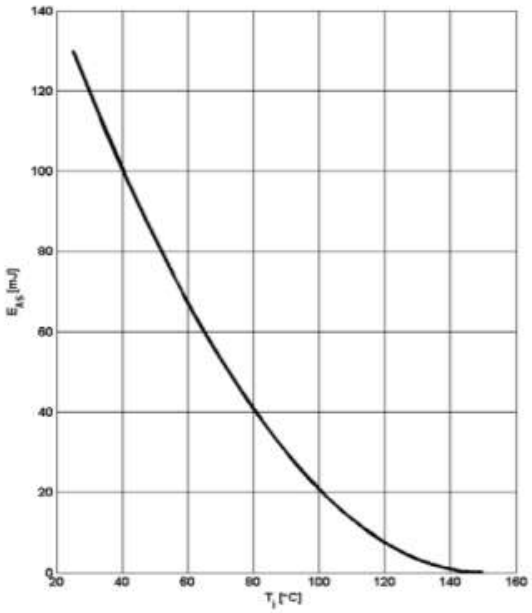


3. Unclaimed Inductive Switching Test Circuit & Waveforms



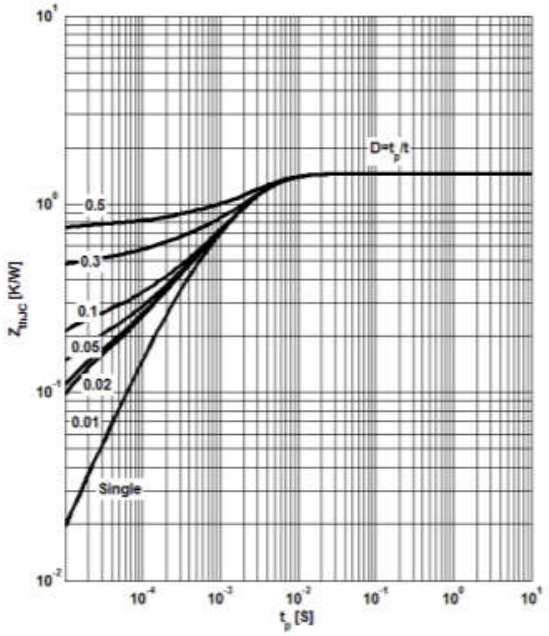
Typical Characteristics

Figure 3: Power Dissipation



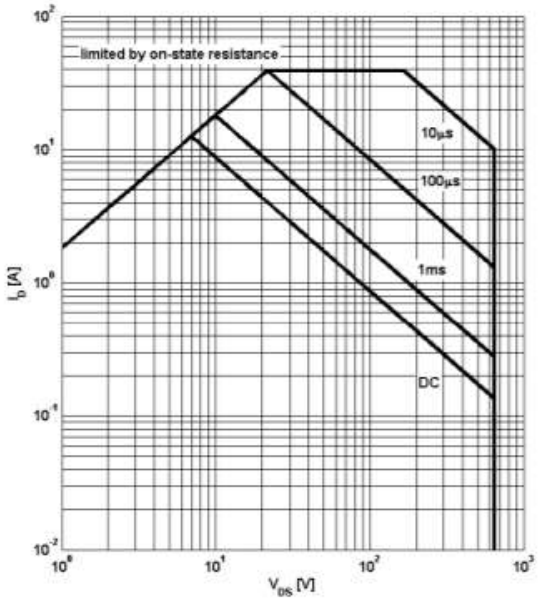
$P_{tot} = f(T_c)$

Figure 4: Max. Transient Thermal Impedance



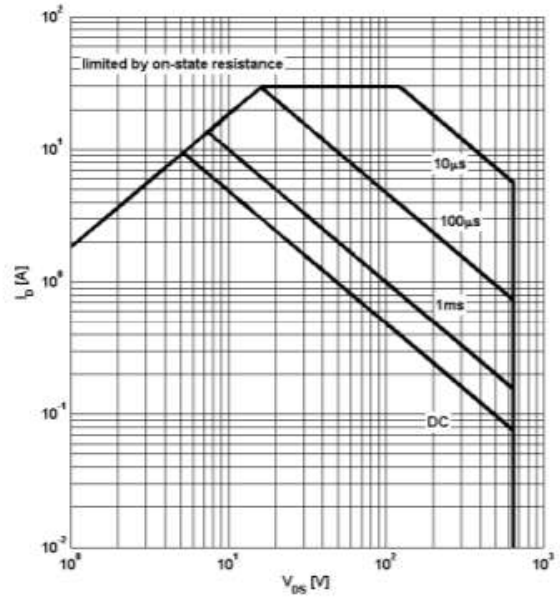
$Z(_{thJC}) = f(t_p)$; parameter: $D = t_p/T$

Figure 5: Safe Operating Area



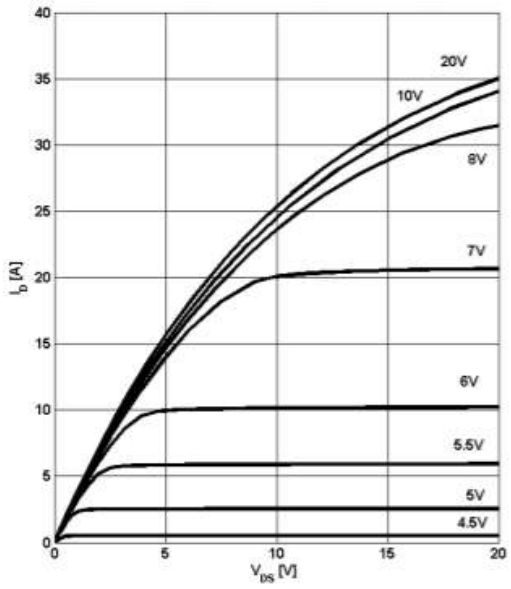
$I_D = f(V_{DS})$; $T_c = 25°C$; $V_{GS}>7V$; parameter t_p

Figure 6: Safe Operating Area



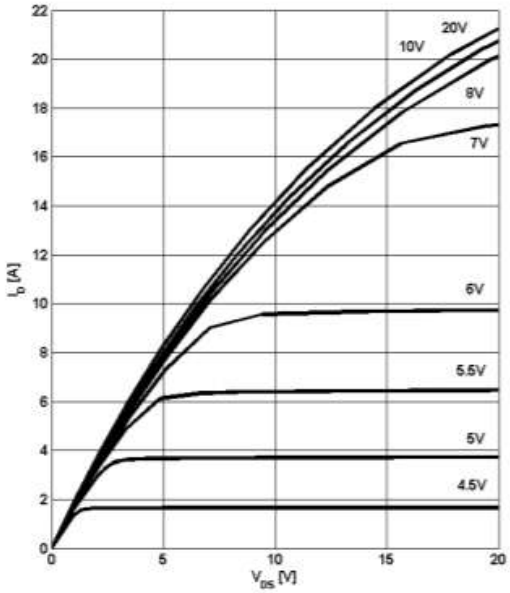
$I_D = f(V_{DS})$; $T_c = 80°C$; $V_{GS}>7V$; parameter t_p

Figure 7: Typ. Output Characteristics



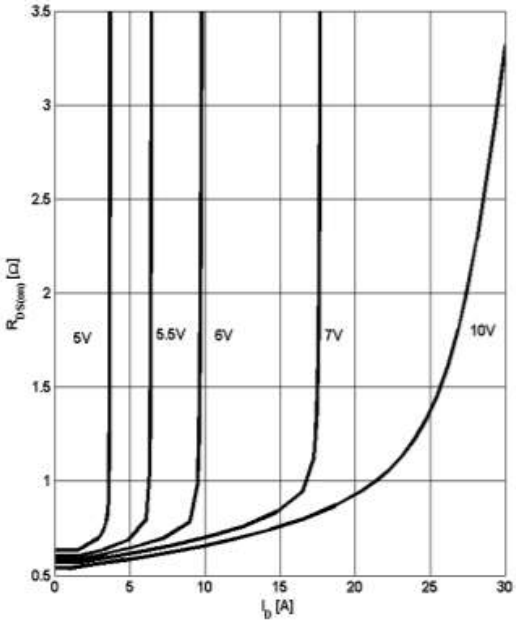
$I_D = f(V_{DS})$; Tj= 25°C; parameter: V_{GS}

Figure 8: Typ. Output Characteristics



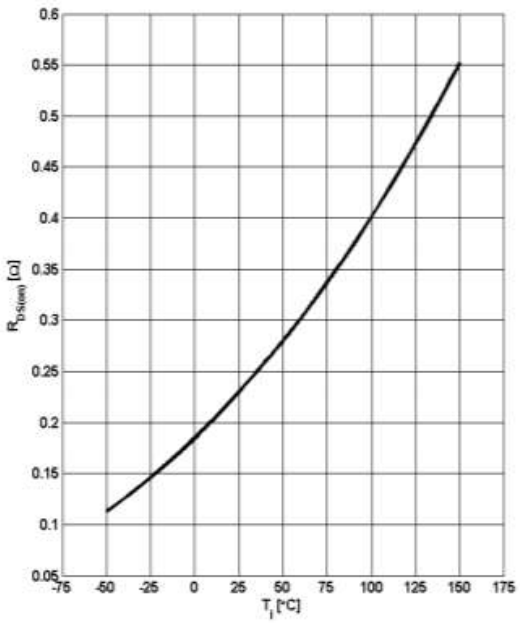
$I_D = f(V_{DS})$; T_j= 125°C; parameter: V_{GS}

Figure 9: Typ. Drain-Source On-State Resistance



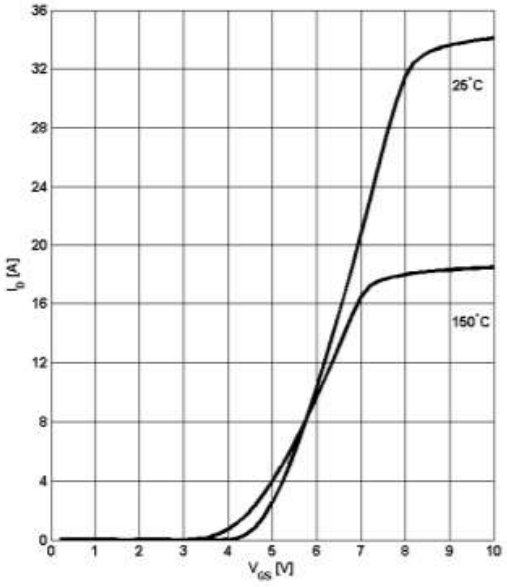
$R_{DS(ON)} = f(I_D)$; T_j=125°C; parameter: V_{GS}

Figure 10: Typ. Drain-Source On-State Resistance



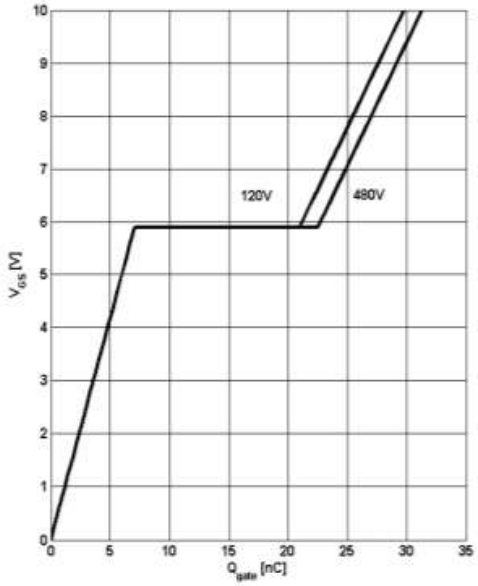
$R_{DS(ON)} = f(T_j)$; I_D=7.0A; V_{GS}=10V

Figure 11: Typ. Transfer Characteristics



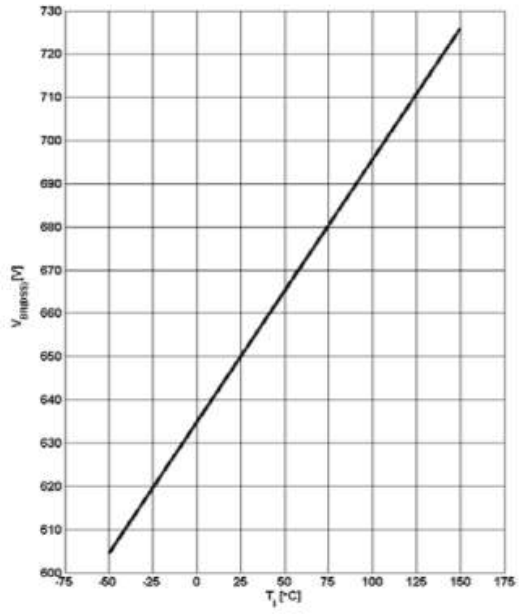
$I_D = f(V_{GS})$; $V_{DS} = 20V$

Figure 12: Typ. Gate Charge



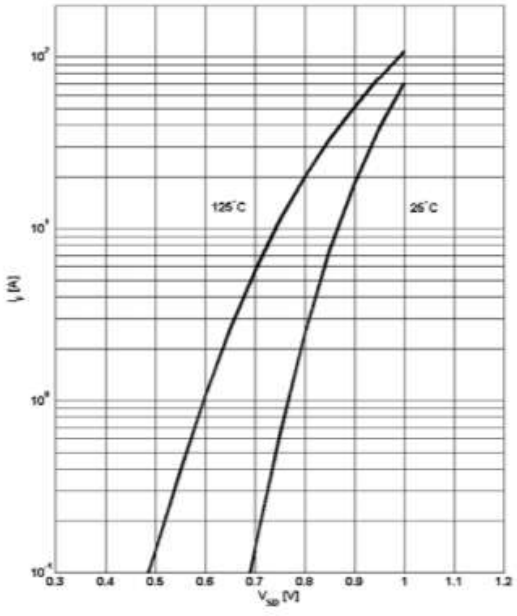
$V_{GS} = f(Q_{gate})$, $I_D = 5.0A$ pulsed

Figure 13: Drain-Source Breakdown Voltage



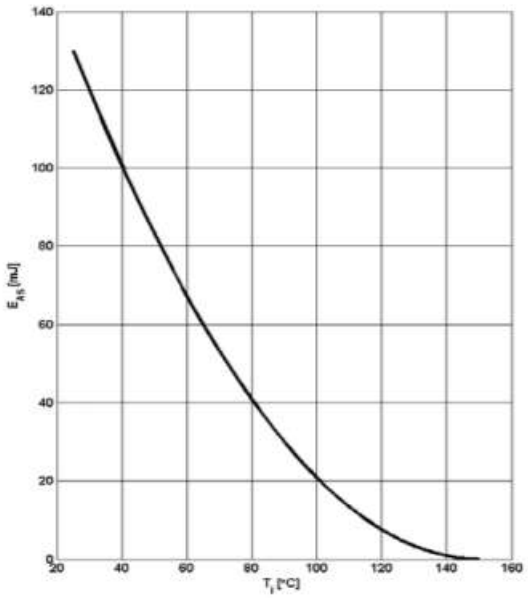
$V_{BR(DSS)} = f(T_j)$; $I_D = 1mA$

Figure 14: Forward Characteristics of Reverse Diode



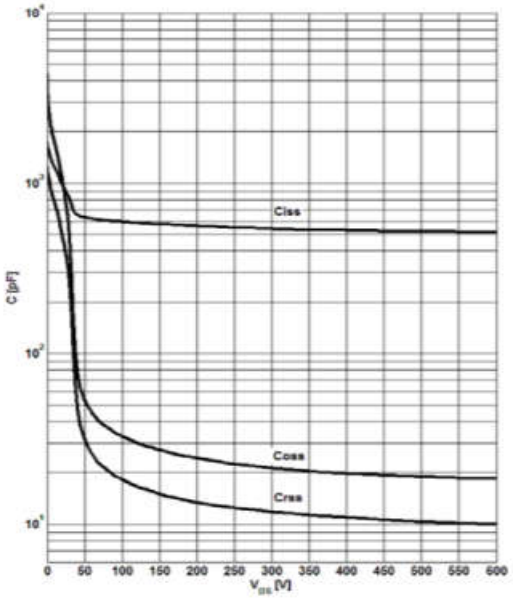
$I_F = f(V_{SD})$; parameter: T_j

Figure 15: Avalanche Energy



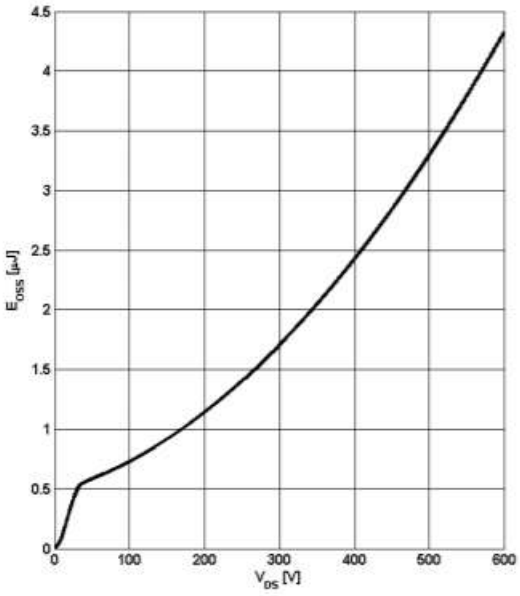
$E_{AS}=f(T_j)$; $I_D=1.7A$; $V_{DD}=60V$

Figure 16: Typ. Capacitances



$C=f(V_{DS})$; $V_{GS}=0$; f=1MHz

Figure 17: C_{OSS} Stored Energy



$E_{OSS}=f(V_{DS})$