



GL120N50A47PFD

Silicon N-Channel Power MOSFET Integrated FRD

General Description:

GL120N50A47PFD, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247PLUS, which accords with the RoHS standard.

Features: Ø

- Fast Switching
- ESD Improved Capability
- Low Gate Charge (Typical Data: 280nC)
- Low Reverse transfer capacitances(Typical: 160pF)
- 100% Single Pulse avalanche energy Test

Applications:

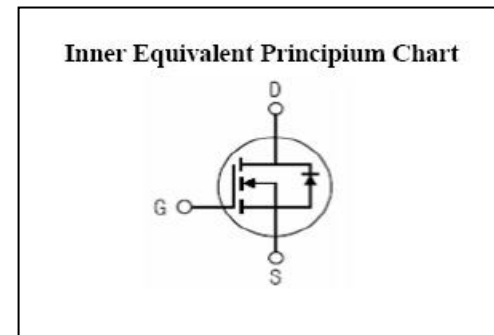
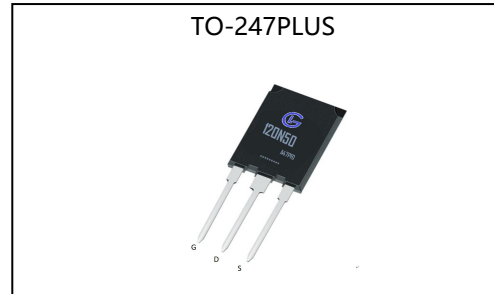
- Power switch circuit of PC POWER

Absolute (Tc=25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage	500	V
I _D	Continuous Drain Current	120	A
	Continuous Drain Current T _C =100 °C	84	A
I _{DM} ^{a1}	Pulsed Drain Current	300	A
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS}	Single Pulse Avalanche Energy	4	J
E _{Ar} ^{a1}	Avalanche Energy ,Repetitive	800	mJ
I _{AR} ^{a1}	Avalanche Current	120	A
dv/dt ^{a2}	Peak Diode Recovery dv/dt	5.0	V/ns
P _D	Power Dissipation	961	W
	Derating Factor above 25°C	7.688	W/°C
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	300	°C

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

V _{DSS} (T _C =150°C)	500	V
I _D	120	A
P _D (T _C =25°C)	961	W
R _{DS(ON)}	40	mΩ





GL120N50A47PFD

Silicon N-Channel Power MOSFET Integrated FRD

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.13	°C/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	20	°C/ W

Electrical Characteristics (T_c= 25°C unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	500	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=500V, V_{GS}=0V, T_a=25^\circ C$	--	--	10	μA
		$V_{DS}=400V, V_{GS}=0V, T_a=125^\circ C$	--	--	1000	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	2100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-200	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=60A$	--	40	45	m Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	V
g_{fs}	Forward Trans conductance	$V_{DS}=30V, I_D=60A$	--	100	--	S

Pulse width < 380 μ s; duty cycle < 2%.

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	--	18000	--	pF
C_{oss}	Output Capacitance		--	1450	--	
C_{rss}	Reverse Transfer Capacitance		--	160	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=60A, V_{DD}=250V$ $V_{GS}=10V, R_g=25\Omega$	--	69	--	ns
t_r	Rise Time		--	125	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	488	--	
t_f	Fall Time		--	150	--	
Q_g	Total Gate Charge	$I_D=60A, V_{DD}=250V$ $V_{GS}=10V$	--	280	--	nC
Q_{gs}	Gate to Source Charge		--	50	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	80	--	



GL120N50A47PFD

Silicon N-Channel Power MOSFET Integrated FRD

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	120	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	300	A
V_{SD}	Diode Forward Voltage	$I_S=100A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=60A, T_j=25^\circ C$	--	90	150	ns
Q_{rr}	Reverse Recovery Charge	$di_f/dt=100A/\mu s, V_{GS}=0V$	--	2.80	--	μC

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $I_{SD}=100A, di/dt \leq 100A/\mu s, V_{DD} \leq BV_{DS}, \text{ Start } T_j=25^\circ C$



GL120N50A47PFD

Silicon N-Channel Power MOSFET Integrated FRD

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

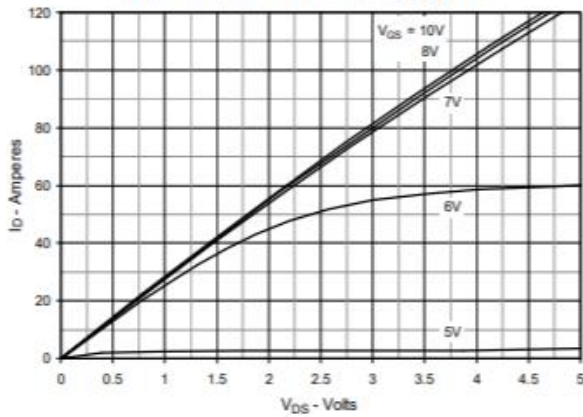


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

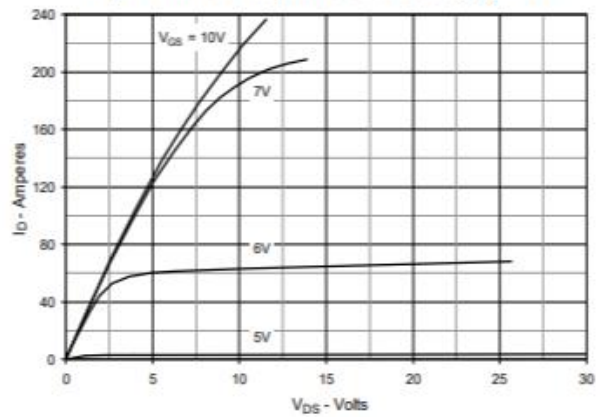


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

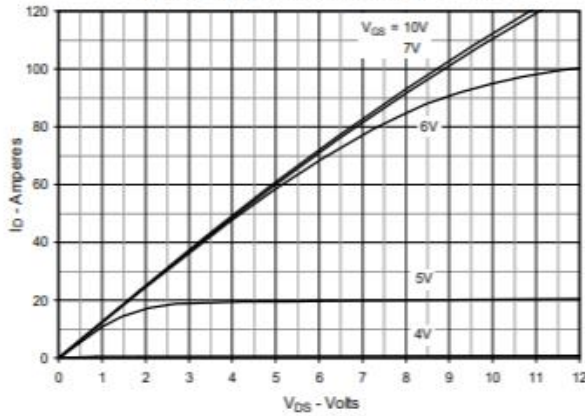


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 60\text{A}$ Value vs. Junction Temperature

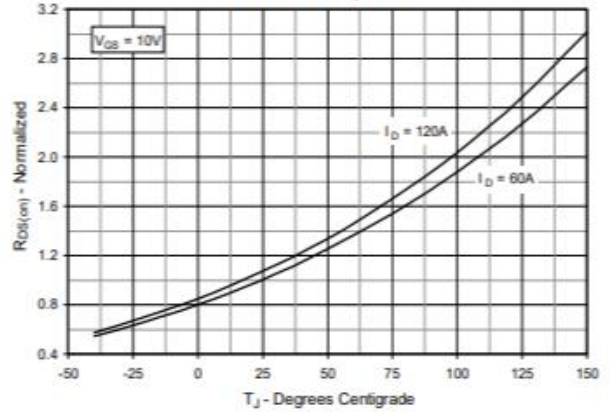


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 60\text{A}$ Value vs. Drain Current

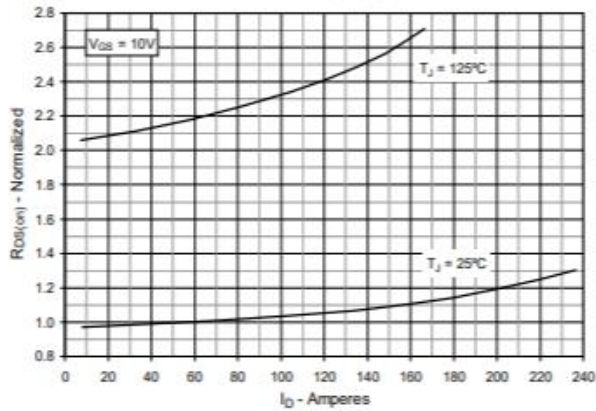
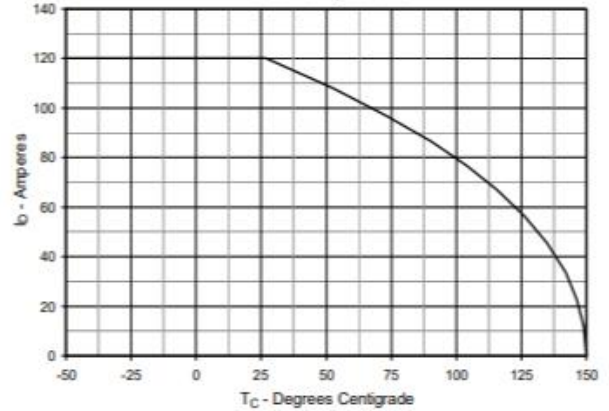


Fig. 6. Maximum Drain Current vs. Case Temperature





GL120N50A47PFD

Silicon N-Channel Power MOSFET Integrated FRD

Fig. 7. Input Admittance

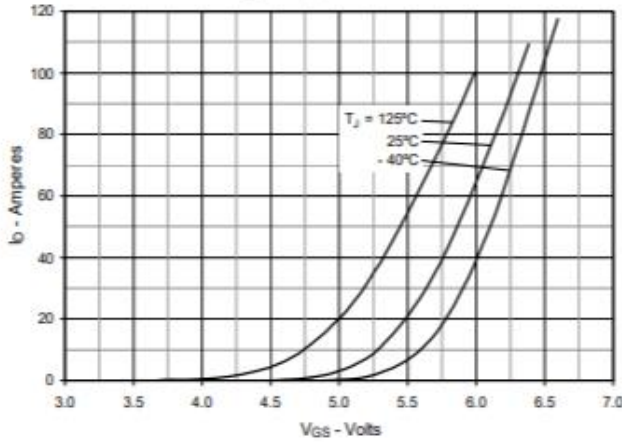


Fig. 8. Transconductance

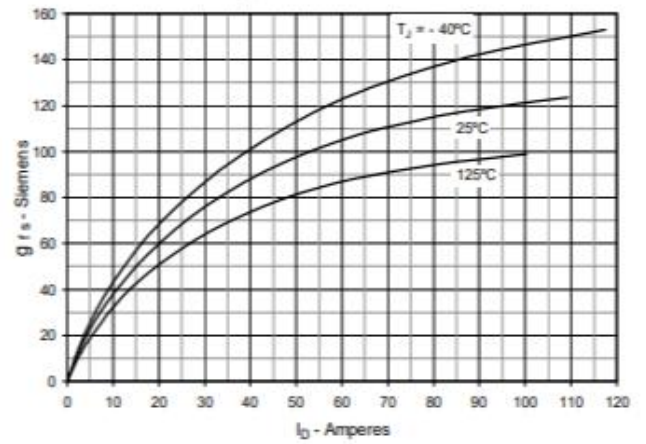


Fig. 9. Forward Voltage Drop of Intrinsic Diode

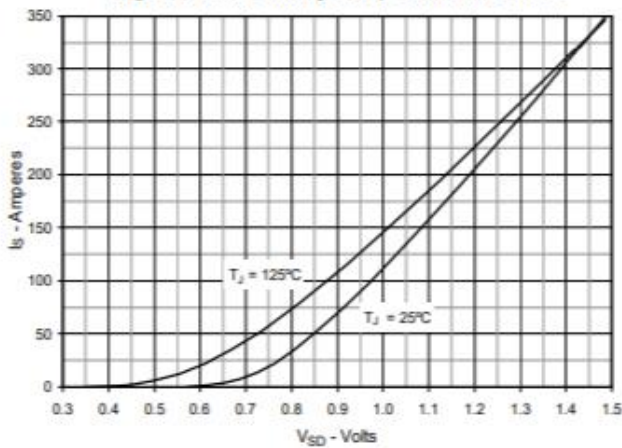


Fig. 10. Gate Charge

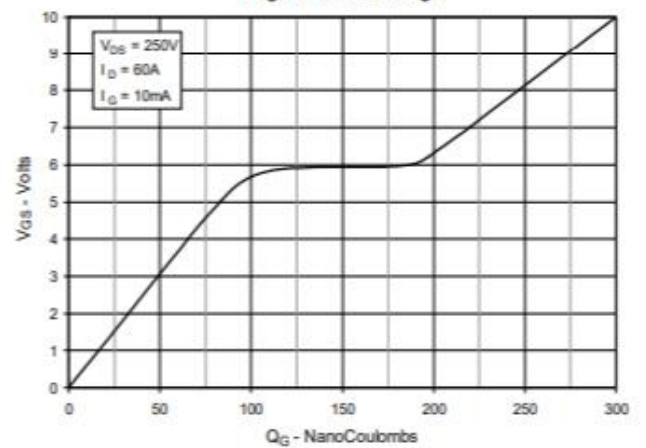


Fig. 11. Capacitance

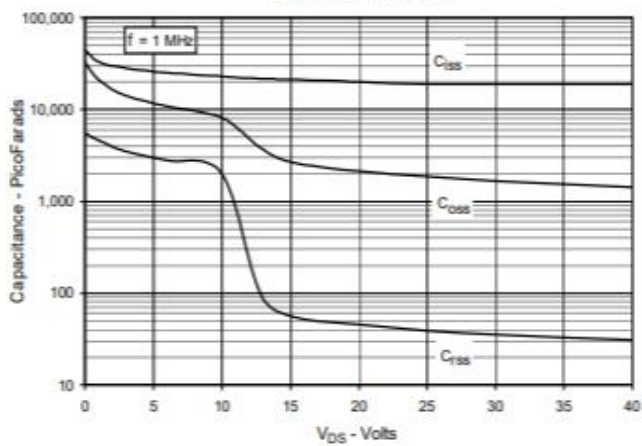
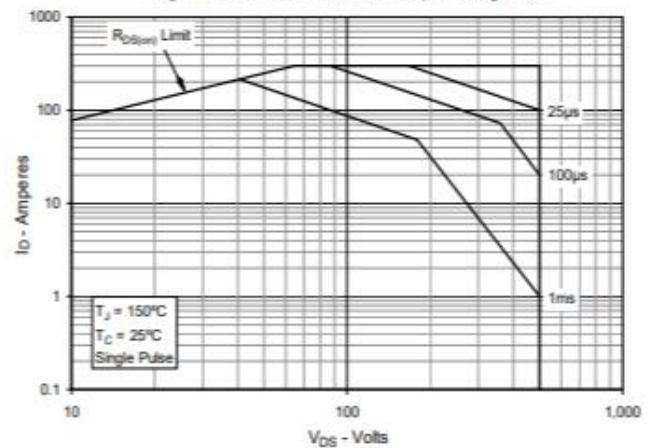


Fig. 12. Forward-Bias Safe Operating Area





GL120N50A47PFD

Silicon N-Channel Power MOSFET Integrated FRD

Fig. 13. Maximum Transient Thermal Impedance

